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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/670,231	09/28/2000	John S. Sadowsky	INTL-0328-US (P8031)	7225
21906	7590	09/13/2006	EXAMINER	
TROP PRUNER & HU, PC 1616 S. VOSS ROAD, SUITE 750 HOUSTON, TX 77057-2631			CHAUDRY, MUJTABA M	
			ART UNIT	PAPER NUMBER
			2133	

DATE MAILED: 09/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

### Application No.

09/670,231

### Applicant(s)

SADOWSKY, JOHN S.

### Examiner

Mujtaba K. Chaudry

### Art Unit

2133

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 21 June 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-12 and 21-26 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-6 and 21 is/are rejected.
- 7) ☒ Claim(s) 7-12 and 22-26 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)   | 5) <input type="checkbox"/> Notice of Informal Patent Application                       |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)<br>Paper No(s)/Mail Date <u>4/29/2004</u> . | 6) <input type="checkbox"/> Other: _____  |

### **DETAILED ACTION**

Applicants' response was received June 21, 2004.

- Claims 1-12 and 21-26 remain.
- Claims 1-6 and 21 remain rejected.
- Claims 7-12 and 22-26 remain objected.
- IDSs filed April 29, 2004, October 5, 2005 and January 20, 2006 have been received and considered.
- Claim objections and rejections under 35USC112 are withdrawn.

Application pending.

### ***Response to Amendment***

Applicant's arguments/amendments with respect to previously presented claims 1-12 and 22-26 and currently amended claim 21 filed June 21, 2004 have been received and considered. All arguments have been fully considered but are not persuasive. The Examiner would like to point out that this action is made final (See MPEP 706.07a).

Applicant contends, "...Marakami (prior art of record) does not teach or suggest that the host processor 403 to perform an operation scheduled by the signal processor 404." The Examiner respectfully disagrees. Marakami teaches (Figure 38 and corresponding text) that, "when the content of a process to be executed by the signal processor 404 needs to be changed, the host processor 403 gives the signal processor 404 the hold request signal 405 requesting the temporary stop of instruction word execution. Upon the end of an instruction presently being

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executed after the reception of the hold request signal 405, **the signal processor 404 provides the hold authorizing signal 406 to stop updating the PC 407 and to interrupt the execution of the instruction word temporarily.**” Therefore, in accordance with MPEP 2111, Marakami teaches the host processor to perform an operation which is directed by the signal processor.

The Examiner disagrees with the Applicant and maintains rejections with respect to claims 1-6 and 21. All arguments have been considered. It is the Examiner’s conclusion that claims 1-6 and 21, as presented, are not patentably distinct or non-obvious over the prior art of record, nor do they incorporate the novelty of the present application. Prior action:

***Allowable Subject Matter***

Claim 22 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Furthermore, dependent claims 7-12 and 23-26 would be allowable as well if the limitations of claims 22 are incorporated within claims 1 and 21. Reasons for indicating allowable subject matter:

Dependent Claim 22 teaches the system comprising a digital signal processor having a bus connected to a memory, a data address generator and an arithmetic unit and a butterfly coprocessor, wherein the digital signal processor has a software program which causes the system to identify a stage of a trellis diagram with the number of nodes in each stage with the number of branches extending from each node. The prior art of record, namely Murakami et al. (herein after: Murakami) teaches a digital signal processor of a simple circuit configuration

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capable of implementing arithmetic processes and interruption processes efficiently in a reduced number of steps at a high processing speed. The digital signal processor comprises instruction execution pipeline stages including a stage in which data is read from a data memory and the data is applied to an arithmetic unit; an arithmetic unit for the execution stage, including a barrel shifter, a multiplier and an arithmetic and logic unit, a normalizing barrel shifter, a round-off/accumulation adder, internal data memories and a DMA transfer bus for a write/accumulation stage, an address generating unit capable of parallel and two-dimensional generation of two inputs one output data memory addresses and a DMA control unit for controlling the two-dimensional data transfer through a DMA bus between the internal data memories and an external data memory for an instruction execution stage. In particular, Murakami teaches (Figure 38) system comprising a digital signal processor (404) coupled to an external memory (413) and a host processor (403), which is analogous to the butterfly coprocessor of the present application. Furthermore, Murakami teaches a data address generator and a arithmetic unit to be incorporated within the program counter (407). However, Murakami fails to teach a digital signal processor having a bus connected to a memory, a data address generator and a arithmetic unit and a butterfly coprocessor, wherein the **digital signal processor has a software program which causes the system to identify a stage of a trellis diagram with the number of nodes in each stage with the number of branches extending form each node.** [Emphasis added] Therefore, the prior art does not fairly teach nor suggest to teach the limitations as suggested by those of claim 22.

***Claim Rejections - 35 USC § 103***

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35

U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1-6 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Murakami et al. (USPN 5045993).

As per claims 1 and 21, Murakami et al. (herein after: Murakami) substantially teaches (title and abstract) a digital signal processor of a simple circuit configuration capable of implementing arithmetic processes and interruption processes efficiently in a reduced number of steps at a high processing speed. The digital signal processor comprises instruction execution pipeline stages including a stage in which data is read from a data memory and the data is applied to an arithmetic unit; an arithmetic unit for the execution stage, including a barrel shifter, a multiplier and an arithmetic and logic unit, a normalizing barrel shifter, a round-off/accumulation adder, internal data memories and a DMA transfer bus for a write/accumulation stage, an address generating unit capable of parallel and two-dimensional generation of two inputs one output data memory addresses and a DMA control unit for controlling the two-dimensional data transfer through a DMA bus between the internal data memories and an external data memory for an instruction execution stage. In particular, Murakami teaches (Figure 38) system comprising a digital signal processor (404) coupled to an external memory (413) and

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a host processor (403), which is analogous to the butterfly coprocessor of the present application. Furthermore, Murakami teaches a data address generator and an arithmetic unit to be incorporated within the program counter (407).

Murakami does not explicitly teach the coprocessor or the host processor (403) to be a butterfly coprocessor as stated in the present application.

However, the present application defines the coprocessor (specification, page 17, lines 24-28) the butterfly coprocessor to perform add-compare-select functions. In the reference, Murakami teaches, referring to Figure 38, a host processor 403, a signal processor 404, a hold request signal 405 requesting the temporary stop of instruction execution of the signal processor 404, a hold authorizing signal 406 for informing an external unit of the temporary stop of the signal processor 404, a program counter (PC) 407, an instruction memory control unit 408, a reloadable writable instruction memory 409, an instruction address 410, a switching circuit 411, a selection signal 412, an external instruction memory 413, instruction words 414 and 415, a comparing circuit 416, a result 417 of decision, and write end signal 418. The signal processor 404 has an arithmetic unit the same as that of the conventional signal processor, and hence the arithmetic unit is not shown in FIG. 38. In Figure 39, Murakami teaches a flow chart of in explaining the operation of the signal processor. When the content of a process to be executed by the signal processor 404 needs to be changed, the host processor 403 (analogous to butterfly coprocessor) gives the signal processor 404 the hold request signal 405 requesting the temporary stop of instruction word execution. Upon the end of an instruction presently being executed after the reception of the hold request signal 405, the signal processor 404 provides the hold authorizing signal 406 to stop updating the PC 407 and to interrupt the execution of the

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instruction word temporarily. Then, the instruction memory control unit 408 provides the instruction address 410 specifying an address to be reloaded in the writable instruction memory 409, and the selection signal 412 to control the switching circuit 411 so that the instruction address 410 is selected. At the same time, the instruction address 410 is given also to the external instruction memory 413. Then, the external instruction memory 413 provides an instruction word 414, which is written in the writable instruction memory 409. The instruction word 414 is written in the writable instruction memory 409 is read from the writable instruction memory 409. The instruction word 415 read from the rewritable instruction memory 409 and the instruction word 414 written in the same are compared by the comparison circuit 416 to decide whether or not the instruction words 414 and 415 coincide with each other. When the instruction word 414 is not written correctly in the rewritable instruction memory 409, the two instruction words do not coincide with each other. Then, a write error flag is set according to the result 417 of decision in the instruction memory control unit 408. This write error signal is not reset until all the write operations are completed. Thus, operation for writing one instruction word is completed. This operation is repeated until all the instruction words are rewritten. After all the instruction words have been rewritten, the status of the write error flag is examined. When the write error flag is set, the instruction word write operation is restarted after resetting the write error flag. When any write error flag is not set and the rewrite has been ended normally, a write end signal 418 is given to the host processor 403. Then, the host processor cancels the hold request signal 405 to cancel the temporary stop mode. Upon the cancellation of the hold request signal 405, the instruction memory control unit 408 of the signal processor 404 provides a selection signal 412 to make the switching circuit 411 select the instruction address of the PC



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407, the instruction address of the PC 407 is updated, and then an instruction at an instruction address succeeding the instruction address of the last instruction word executed before the execution of instructions was stopped temporarily is executed. Thus the contents of the signal processing process can readily be changed by providing the signal processor with an internal rewritable instruction memory. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate a butterfly coprocessor within the method and apparatus of Murakami. This modification would have been obvious to one of ordinary skill in the art because one of ordinary skill would have recognized that by replacing the host processor with a butterfly coprocessor would increase the efficiency of the system by performing high-speed butterfly operations.

As per claim 2, Murakami substantially teaches, in view of above rejections, (col. 50, lines 21-34) a digital signal processor which includes data address generator coupled to a bus.

As per claim 3, Murakami substantially teaches, in view of above rejections, (col. 49, lines 44-47) an arithmetic logic unit capable of processing the input data at least through addition, subtraction and absolute differential operation within one machine cycle.

As per claims 4-6, Murakami substantially teaches, in view of above rejections, (col. 9, lines 10-64) a conditional branch instruction is an instruction to specify executing an instruction word in a branched address specified by the instruction when the specified branch condition is met or to specify executing an instruction word in the next address. When the conditional branch instruction is decoded, a flag 69A held by the flag register 69 is read and is applied to a condition decision unit 72. The condition decision unit 72 decides whether or not the branch condition 64A specified by the instruction is met. When the branch condition 64A is met, the logical value

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of a branch signal 72A becomes "1", the switching circuit 71 selects the branched address 64B specified by an instruction, and then the branched address 64B is given to the PC 61. When the branch condition 64A is not met, the logical value of the branch signal 72A becomes "0", the switching circuit 71 selects the address 71A greater than the instruction address 70A by "1", and then the address 71A is given to the PC 61. Operation of the processor in a case where only information indicating whether or not  $A=B$  (A and B are input data) is met is required will be described with reference to FIG. 7. First data A0 and B0 are compared. When the data A0 is equal to the data B0, the value of a predetermined address TS(0) in the data memory is made "1". When the data A.sub.0 is not equal to the data B0, the value of the address TS(0) is made "0". Then, data A.sub.1 and B.sub.1 are compared and the result of the comparison is written at an address TS(1). The result of comparison of data A.sub.2 and B.sub.2 is written at an address TS(2).


***Conclusion***

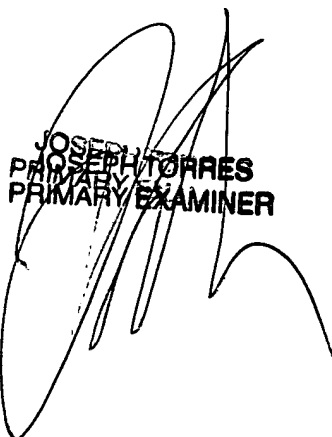
**THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiries concerning this communication should be directed to the examiner, Mujtaba Chaudry who may be reached at 571-272-3817. The examiner may normally be reached Mon – Thur 6:30 am to 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, please contact the examiner's supervisor, Albert DeCady at 571-272-3819.

  
Mujtaba Chaudry  
Art Unit 2133  
September 7, 2006

  
JOSEPH TORRES  
PRIMARY EXAMINER